NEW UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Docket No. M4065.0244/P244
Total pages in this submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD AND APPARATUS FOR ADJUSTING DATA HOLD TIMING OF AN OUTPUT CIRCUIT

and invented by:

James S. Cullum and Steven Renfro

IF A CONTINUATION APPLICATION, check appropriate box and supply requisite information:

☐ Continuation ☐ Divisional

☐ Continuation-in-part (CIP) of prior application No.: _____

Enclosed are:

Application Elements

1. [X] Filing fee as calculated and transmitted as described below
2. [X] Specification having 20 pages(s) and including the following:
   a. [X] Descriptive title of the invention
   b. [ ] Cross references to related applications *(if applicable)*
   c. [ ] Statement regarding Federally-sponsored research/development *(if applicable)*
   d. [ ] Reference to microfiche appendix *(if applicable)*
   e. [X] Background of the invention
   f. [X] Brief summary of the invention
   g. [X] Brief description of the drawings *(if drawings filed)*
   h. [X] Detailed description
   i. [X] Claims as classified below
   j. [X] Abstract of the disclosure

Application Elements (continued)

3. [X] Drawing(s) *(when necessary as prescribed by 35 U.S.C. 113)*

   [ ] Formal [X] Informal Number of sheets: 5

4. [X] Oath or Declaration

   a. [X] Newly executed (original or copy) [ ] Unexecuted

   b. [ ] Copy from a prior application (37 C.F.R. 1.63(d) *(for continuation/divisional applications only)*

   c. [ ] With Power of Attorney [X] Without Power of Attorney

5. [ ] Incorporation by reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Computer program in microfiche

7. [ ] Genetic sequence submission *(if applicable, all must be included)*

   a. [ ] Paper copy

   b. [ ] Computer readable copy

   c. [ ] Statement verifying identical paper and computer readable copies

Accompanying Application

8. [X] Assignment papers *(cover sheet & document(s))*

9. [X] 37 C.F.R. 3.73(b) statement *(when there is an assignee)*

10. [ ] English translation document *(if applicable)*

11. [ ] Information Disclosure Statement/PTO-1449 [ ] Copies of IDS citations

12. [ ] Preliminary Amendment

13. [X] Acknowledgment postcard

14. [ ] Certified copy of priority document(s) *(if foreign priority is claimed)*

15. [ ] Certificate of Mailing

    [ ] First Class [ ] Express Mail (Label No.: _____)

16. [ ] Small Entity statement(s) -- # submitted _____ *(if Small Entity status claimed)*

Accompanying Application (continued)

17. ☐ Additional enclosures *(please identify below):*

Fee Calculation and Transmittal

The filing fee for this utility patent application is calculated and transmitted as follows:

☒ Large Entity ☐ Small Entity

CLAIMS AS FILED					
For	**# Filed**	**# Allowed**	**# Extra**	**Rate**	**Fee**
Total Claims	48	- 20 =	28	x $18.00	$504.00
Independent Claims	4	- 3 =	1	x $78.00	$78.00
Multiple Dependent Claims (check if applicable)			☐		
Other Fees (specify purpose): Recordation Form Cover Sheet					$40.00
				BASIC FEE	$690.00
				TOTAL FILING FEE	$1,312.00

☒ A check in the amount of $1,312.00 to cover the total filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and Deposit Account No. 4 - 1073 as described below. A duplicate copy of this sheet is enclosed.

☐ Charge the amount of _____ as filing fee.

☒ Credit any overpayment.

☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.

☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).

Dated: May 22, 2000

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Micron Ref No. : 99-0700

Docket No.: **M4065.0244/P244**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR U.S. LETTERS PATENT

Title:

METHOD AND APPARATUS FOR ADJUSTING DATA HOLD TIMING OF AN OUTPUT CIRCUIT

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METHOD AND APPARATUS FOR ADJUSTING tOH TIMING OF AN OUTPUT CIRCUIT

Field of the Invention

The present invention relates to method and apparatus for adjusting the timing of data availability at an output buffer of a digital circuit and more particularly to a method and apparatus for individually adjusting the data hold timing of each output buffer circuit for a multi-bit data path.

Background of the Invention

FIG. 1 illustrates a conventional output circuit for a digital circuit. To simplify discussion, this application will assume that the digital circuit is a memory circuit; however, it should be understood that the invention described herein applies to any circuit which outputs data. Data lines 11a, 11b...11n each receive a respective data bit DQ0, DQ1...DQn from a memory core, and provide the respective data bits to respective output buffer latches 13a, 13b...13n which in turn deliver the latched output data DQ0, DQ1...DQn to a plurality of output data lines 15a, 15b...15n. The output buffer latches 13a, 13b...13n are clocked by a clock signal which originates from a clock source 17 and is provided to the output buffer latches 13a, 13b...13n in common, either directly from clock source 17, or through a delay circuit 19. The clock signal applied to the output buffer latches 13a, 13b...13n causes the output buffers to

latch in data from the data lines 11a, 11b...11n and make it available on the output lines 15a, 15b...15n for a period of time know as the data hold time, commonly referred to as t_{oh}.

As shown in FIG. 2 a first clock cycle is used to synchronize a READ operation which causes the data DQ0, DQ1...DQn to be delivered from a memory core to the lines 11a, 11b...11n and a subsequent clock cycle T_1 causes the output buffers to latch and hold the data on lines 11a, 11b...11n for the data hold time. The time the data DQ0, DQ1...DQn is accessed from memory locations and during which it is made available on lines 11a, 11b...11n is commonly referred to as memory access time, t_{ac}.

Referring back to FIG. 1, a delay circuit 19 is often employed to ensure that data is available on all of the data input lines 11a, 11b...11n before the output buffers latch and hold the data.

As the speed of digital circuits continues to increase there are ever increasing demands placed on the timing circuitry for memory devices due to shorter clock periods. In addition, the very complex circuitry of modern digital circuits, e.g., memory devices, often leads to clock signal lines being routed to the output buffer latches 13, 13b...13n with unequal circuit path lengths both inside a chip and/or outside a chip in the chip packaging. As a consequence of these signal path length differences, and other timing aberrations caused by circuit topology within a chip, at

higher clocking speeds, it is becoming increasingly difficult to time align the data across all the output lines 15a, 15b...15c of a memory device.

SUMMARY OF THE INVENTION

The present invention is directed to a data output circuit for digital circuits, for example, memory circuits, which insures that the output data signals DQ0, DQ1...DQn applied to respective data output lines are delivered in substantial coincidence. This is accomplished by individually adjusting the clock signal applied to each of a plurality of output buffer latch circuits 13a, 13b...13n so that the timing of the delivery of the output signals on the output lines can be fine tuned to be substantially coincident, regardless of clock path length differences within a chip and/or within the leads of a chip package.

The invention can also be used to individually adjust the clock signals to respective output buffer circuits to deliver the output data signal DQ0, DQ1...DQn to respective output data lines such that the data signals arrive substantially coincidentally at the output terminals of a packaged digital circuit, for example, a memory circuit.

The invention employs respective adjustable delay circuits in the clock path from a clock source to each of the output buffer latches so that the data hold time tOH for each output buffer latch can be individually adjusted. The amount of delay for each adjustable delay circuit may be programmable .

These and other features and advantages of the invention will be better understood from the following detailed description which is provided in connection with accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a conventional data output circuit;

FIG. 2 illustrates a timing diagram showing operation of the FIG. 1 data output circuit;

FIG. 3 illustrates a data output circuit constructed in accordance with of the invention;

FIG. 4 illustrates the delay control circuit depicted in FIG. 3; and

FIG. 5 illustrates a processor based system which may employ the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 3 illustrates an embodiment of a data output circuit of the invention. Like elements to those in FIG. 1 have the same reference numbers. The FIG. 3 data output circuit permits the data hold time of the output buffer latches 13a, 13b...13n to

be individually adjusted by means of a respective delay control circuits 21a, 21b...21n, each of which delivers a clock signal from a clock source 17 to a respective output buffer latch 13. The delay control circuits 21a, 21b...21n each provide an individually adjustable delay so that the timing of the clock signals delivered from clock source 17 to the respective output buffer latch circuits 13a, 13b...13n can be individually adjusted.

FIG. 4 illustrates an exemplary embodiment of one delay control circuit 21a. It should be understood that each of the delay control circuits 21b...21n in FIG. 3 have an identical construction. Each delay control circuit includes a switch circuit for selecting one of a plurality of delay elements to be used to delay an applied clock signal. The switch circuit is shown in FIG. 4 as a plurality of switch element 23a, 23b...23m. Each switch element 23a, 23b...23m receives the incoming clock signal and is in turn connected to a respective delay element 25a, 25b...25m. The delay elements are each capable of applying a different predetermined delay with respect to an input signal applied thereto. For example, delay element 25a may deliver a .5 nanosecond delay, delay element 25b a 1.0 nanosecond delay and delay element 25m a 1.5 nanosecond delay. It should be apparent from FIG. 4 that although three switch elements 23a, 23b...23m and three associated delay elements 25a, 25b...25m are illustrated that any number of switch elements and delay elements may be used. It should also be apparent that many different types of switch circuits could be used to select one of the delay elements 25a, 25b...25m for delaying the applied clock signal.

As noted, the switch elements 23a, 23b...23m all act as switches and the "on" state of each switch element is controlled by a signal which is applied to it through a respective fuse element or anti-fuse element, 27a, 27b...27m. In practice, one of the fuse or anti-fuse elements 27a, 27b...27m will be "set" relative to the others so that one of the switch elements 23a, 23b...23m is "on" while the rest remain "off." As a consequence, the arriving clock signal DQCLK from clock source 17 which commonly enters each of the switch elements 23a, 23b...23m is passed by the "on" switch to its corresponding delay element 25a, 25b...25m thereby delivering a delayed clock signal DQCLKD to a respective output buffer 13a. The delay control circuit 21a illustrated in FIG. 4 can accordingly be programmed with the fuses or anti-fuses to set a particular clock signal delay for a particular output buffer as desired. The fused or anti-fused devices 27a, 27b...27c can be programmed by the manufacturer, or by a user. If the fuses or anti-fuses are programmed by a manufacturer, the fuses or anti-fuses can be programmed during fabrication and before chip packaging. Alternatively, external pins may be provided on the chip for programming the fuses or anti-fuses by a user.

Returning to the timing diagram of FIG. 2, the delay control circuitry 21a of the invention thus enables the data output circuit of a digital circuit, e.g., a memory circuit, to individually adjust the data hold time of each output buffer to best accommodate the clock signal path characteristics of the digital circuit and/or its packaging. As a result, the data hold times of all output buffers can be made

substantially coincident, either at the output of the buffers or at the output terminals of the digital circuit.

The invention may be easily implemented as part of a digital integrated circuit. The present invention will find particular utility in a digital circuit which uses output buffers to apply data signals to a transmission path, such as a data bus, such as digital circuits employed in a processor based system of the type illustrated in FIG. 5.

As shown in FIG. 5, a processor based system, such as a computer system, generally comprises a central processing unit (CPU) 210, for example, a microprocessor, which communicates with one or more input/output (I/O) devices 240, 250 over a bus 270. The system 200 may also includes random access memory (RAM) 260, a read only memory (ROM) 280 and may include other peripheral devices such as a floppy disk drive 220 and a compact disk (CD) ROM drive 230 which also communicate with CPU 210 over the bus 270. At least one of CPU 210 and one or more integrated circuits connected thereto, such as employed for RAM 260 and ROM 280, may contain the data output circuit described above with reference to FIGS. 3 and 4. It is also possible to integrate the processor 210 and one or more of RAM 260 and ROM 280 on a single IC chip. FIG. 5 is one exemplary processor based architecture with which the invention may be used. Many other processor based architectures are also possible.

While a preferred embodiment of the invention has been described and illustrated above, it should be understood that this is exemplary of the invention and are not to be considered as limiting. Additions, deletions, substitutions, and other modifications can be made without departing from the spirit or scope of the present invention. Accordingly, the invention is not to be considered as limited by the foregoing description, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective first delayed first clock signal to a respective one of said plurality of output circuits.

2. A data output apparatus as in claim 1 wherein each of said output circuits has an associated output data hold time, the timing of which is adjusted by the delay of a respective delay circuit.

3. A data output apparatus as in claim 2 wherein the amount of delay applied by each of said adjustable delay circuits is programmable.

4. A data output apparatus as in claim 2 wherein the delay of each of said adjustable delay circuits is adjusted such that the timing of said data hold time of each of said output circuits is substantially coincident.

5. A data output apparatus as in claim 2 further comprising a plurality of data output terminals respectively connected to said output circuits, and

wherein the delay of each of said adjustable delay circuits is adjusted such that the data hold time as seen at said respective output terminal is substantially coincident.

6. A data output apparatus as in claim 1 wherein each of said delay circuits comprises:

an input for receiving said first clock signal;

a plurality of delay elements, each of said delay elements providing different respective delay to a signal applied thereto; and,

a switch circuit for selectively causing a selected one of said delay elements to delay said first clock signal and apply a delayed first clock signal to a respective output circuit.

7. A data output apparatus as in claim 6 further comprising a programming circuit for programming said switch circuit to selectively apply said first clock signal to one of said delay elements.

8. A data output apparatus as in claim 7 wherein said programming circuit comprises at least one fuse element.

9. A data output apparatus as in claim 7 wherein said programming circuit comprises at lest one anti-fuse element.

10. A data output apparatus as in claim 6 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

11. A data output apparatus as in claim 10 further comprising a programmable circuit for programming which of said switch elements is selectively enabled.

12. A data output apparatus as in claim 1 wherein said output circuits are output buffer circuits.

13. A data output apparatus as in claim 1 wherein each of said output circuits receives and outputs a respective data signal from a memory array.

14. A data output apparatus as in claim 6 wherein said switch circuit comprises at least one multiplexor.

15. A processor based system comprising:

a processor; and

at least one memory circuit coupled to said processor, at least one of said processor and memory circuit including a data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits.

16. A processor based system as in claim 15 wherein each of said output circuits has an associated output data hold time, the timing of which is adjusted by the delay of a respective delay circuit.

17. A processor based system as in claim 16 wherein the amount of delay applied by each of said adjustable delay circuits is programmable.

18. A processor based system as in claim 16 wherein the delay of each of said adjustable delay circuits is adjusted such that the timing of said data hold time of each of said output circuits is substantially coincident.

19. A processor based system as in claim 16 wherein each of said output circuits is coupled to a respective output terminal and the delay of each of said adjustable delay circuits is adjusted such that the data hold time as seen at said respective output terminal is substantially coincident.

20. A processor based system as in claim 15 wherein each of said delay circuits comprises:

an input for receiving said first clock signal;

a plurality of delay elements, each of said delay elements providing a different respective delay to a signal applied thereto; and,

a switch circuit for selectively causing a selected one of said delay elements to delay said first clock signal and apply a delayed first clock signal to a respective output circuit.

21. A processor based system as in claim 20 further comprising a programming circuit for programming said switch circuit to selectively apply said first clock signal to one of said delay elements.

22. A processor based system as in claim 21 wherein said programming circuit comprises at least one fuse element.

23. A processor based system as in claim 21 wherein said programming circuit comprises at lest one anti-fuse element.

24. A processor based system as in claim 21 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

25. A processor based system as in claim 24 further comprising a programmable circuit for programming which of said switch elements is selectively enabled.

26. A processor based system as in claim 15 wherein said output circuits are output buffer circuits.

27. A processor based system as in claim 15 wherein each of said output circuits receives and outputs a respective data signal from a memory array.

28. A processor based system as in claim 20 wherein said switch circuit comprises at least one multiplexor.

29. A memory device comprising:

a memory core; and

a data output apparatus coupled to said memory core and comprising:

a plurality of output circuits each of which receives and outputs a respective data signal from said core, each said output circuit operating in accordance with a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits.

30. A memory device as in claim 29 wherein each of said output circuits has an associated output data hold time, the timing of which is adjusted by the delay of a respective delay circuit.

31. A memory device as in claim 30 wherein the amount of delay applied by each of said adjustable delay circuits is programmable.

32. A memory device as in claim 30 wherein the delay of each of said adjustable delay circuits is adjusted such that the timing of said data hold time of each of said output circuits is substantially coincident.

33. A memory device as in claim 30, further comprising a plurality of data output terminals respectively connected to said output circuits, and

wherein the delay of each of said adjustable delay circuits is adjusted such that the data hold time as seen at said respective output terminal is substantially coincident.

34. A memory device as in claim 29 wherein each of said delay circuits comprises:

an input for receiving said first clock signal;

a plurality of delay elements, each of said delay elements providing different respective delay to a signal applied thereto; and,

a switch circuit for selectively causing a selected one of said delay elements to delay said first clock signal and apply a delayed first clock signal to a respective output circuit.

35. A memory device as in claim 34 further comprising a programming circuit for programming said switch circuit to selectively apply said first clock signal to one of said delay elements.

36. A memory device s in claim 35 wherein said programming circuit comprises at least one fuse element.

37. A memory device as in claim 35 wherein said programming circuit comprises at lest one anti-fuse element.

38. A memory device as in claim 35 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

39. A memory device as in claim 38 further comprising a programmable circuit for programming which of said switch elements is selectively enabled.

40. A memory device as in claim 29 wherein said output circuits are output buffer circuits.

41. A method of providing data output signals comprising:

receiving a plurality of data output signals at respective output circuits; and

operating said output circuits in response to respective applied clock signals to make said data output signals available at the output of said output circuits;

providing a first clock signal; and

generating each said respective applied clock signal from said first clock signal, each said respective applied clock signals having a respective adjustable delay relative to said first clock signal.

42. A method as in claim 41 wherein said data output signals are available at the outputs of said output circuits for a respective data hold time, the timing of said data hold time for each of said output circuits being independently adjusted by adjusting the delay of a respective applied clock signal.

43. A method as in claim 42 wherein the amount of delay of each of said applied clock signals is programmable.

44. A method as in claim 42 further comprising adjusting the delay of each of said applied clock signals such that the timing of said data hold time of each of said output circuits is substantially coincident.

45. A method as in claim 42, wherein each of said output circuits is connected to a respective output terminal, said method further comprising adjusting the delay of said applied clock signals such that the data hold time, as seen at each of said output terminals, is substantially coincident.

46. A method as in claim 45 wherein said terminals are exterior terminals of an integrated circuit package containing said output circuits.

47. A method as in claim 41 wherein each of said applied clock signals is generated by receiving said first clock signal and subjecting said received first clock signal to a selected one of a plurality of signal delays.

48. A method as in claim 47 wherein said selected one of said plurality of signal delays is programmable.

ABSTRACT

A method and apparatus are disclosed for adjusting the individual data hold time of data output buffers. Clock signals for the output buffers are respectively and individually adjusted for each of the output buffers to ensure a desired timing relationship among all of the data output by the buffers.

CLOCK
17
DELAY
19
DQ N
11N
DQ 1
11b
DQ 0
11a
OUTPUT BUFFER LATCH
13N
OUTPUT BUFFER LATCH
13b
OUTPUT BUFFER LATCH
13a
DQ N
15N
DQ 1
15b
DQ 0
15a

Fig. 1

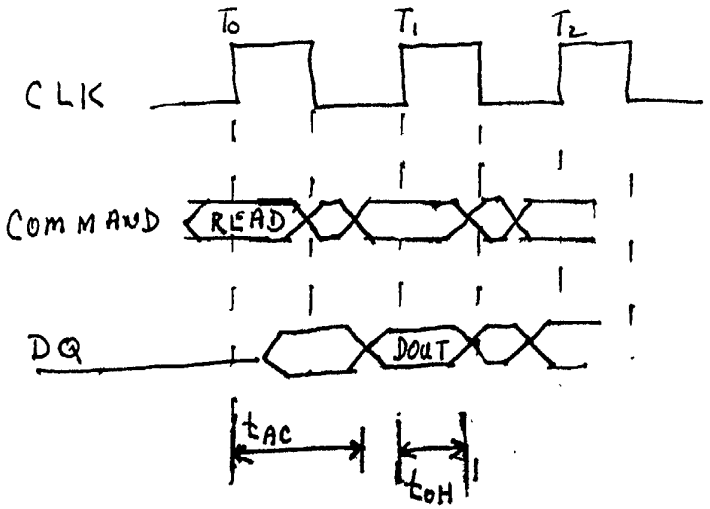

Fig. 2

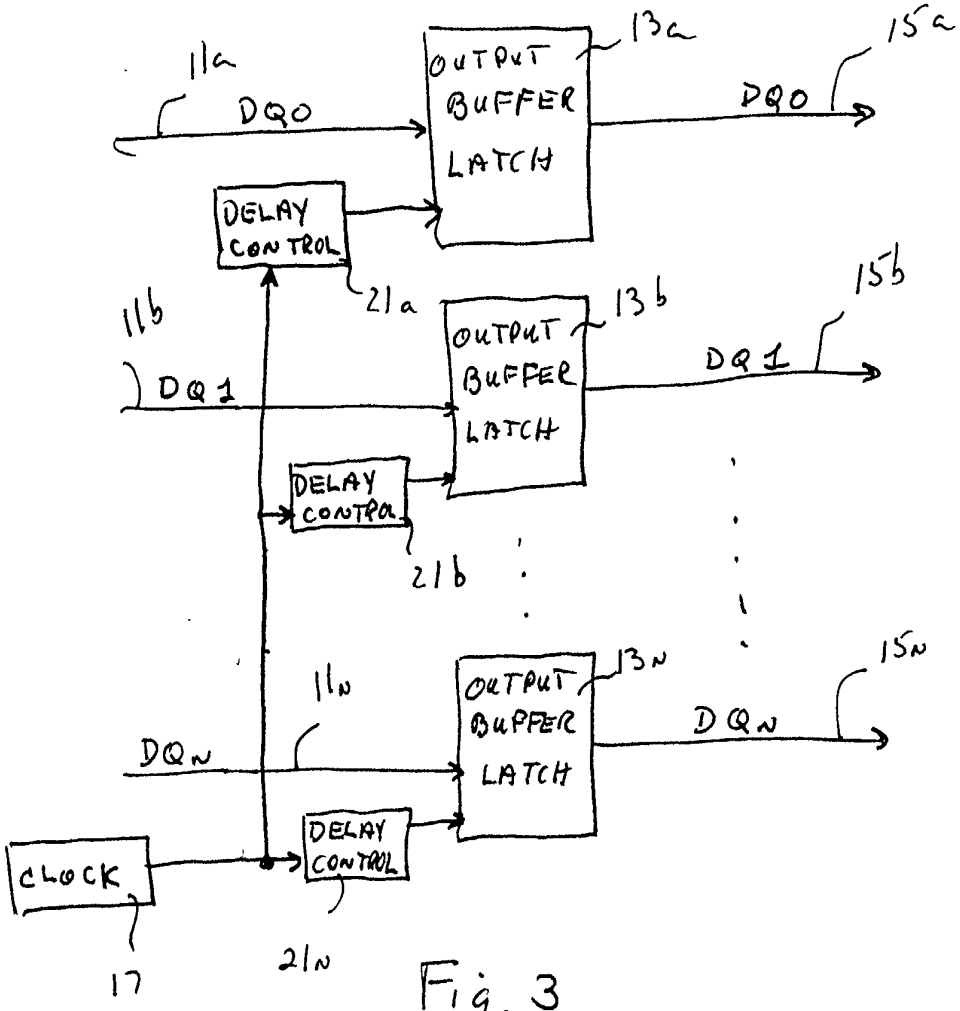
11a
DQ0
OUTPUT BUFFER LATCH
13a
15a
DQ0
DELAY CONTROL
21a
11b
DQ1
OUTPUT BUFFER LATCH
13b
15b
DQ1
DELAY CONTRO
21b
11N
DQN
OUTPUT BUFFER LATCH
13N
15N
DQN
CLOCK
DELAY CONTROL
17
21N

Fig. 3

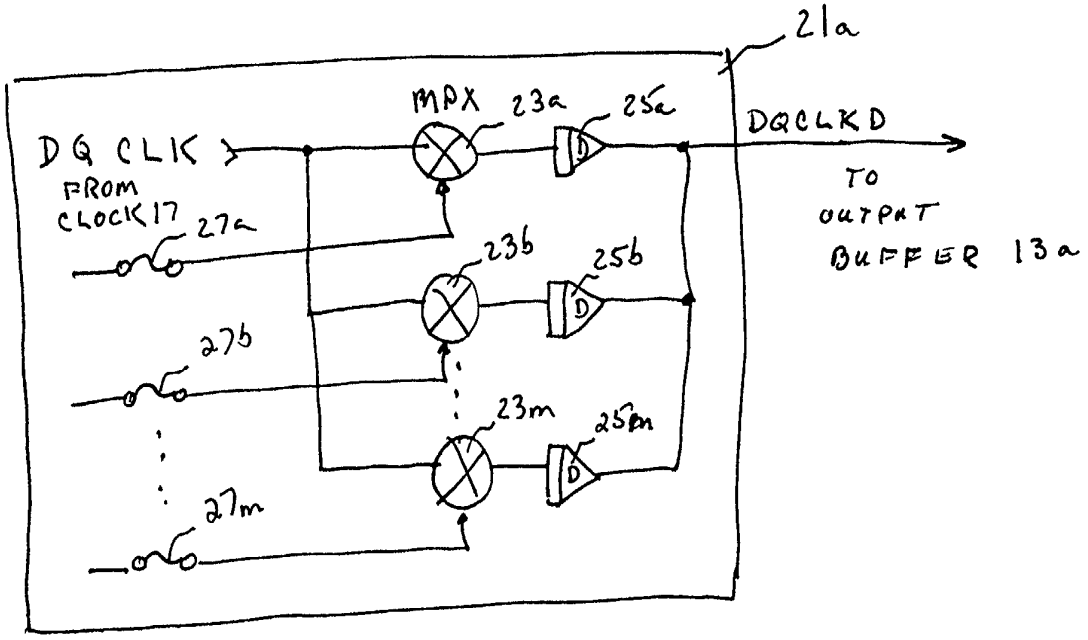
21a
MPX
23a
25a
DQCLK
DQ CLK
FROM
CLOCK 17
TO
OUTPUT
BUFFER 13a
27a
23b
25b
27b
23m
25m
27m
D

Fig. 4

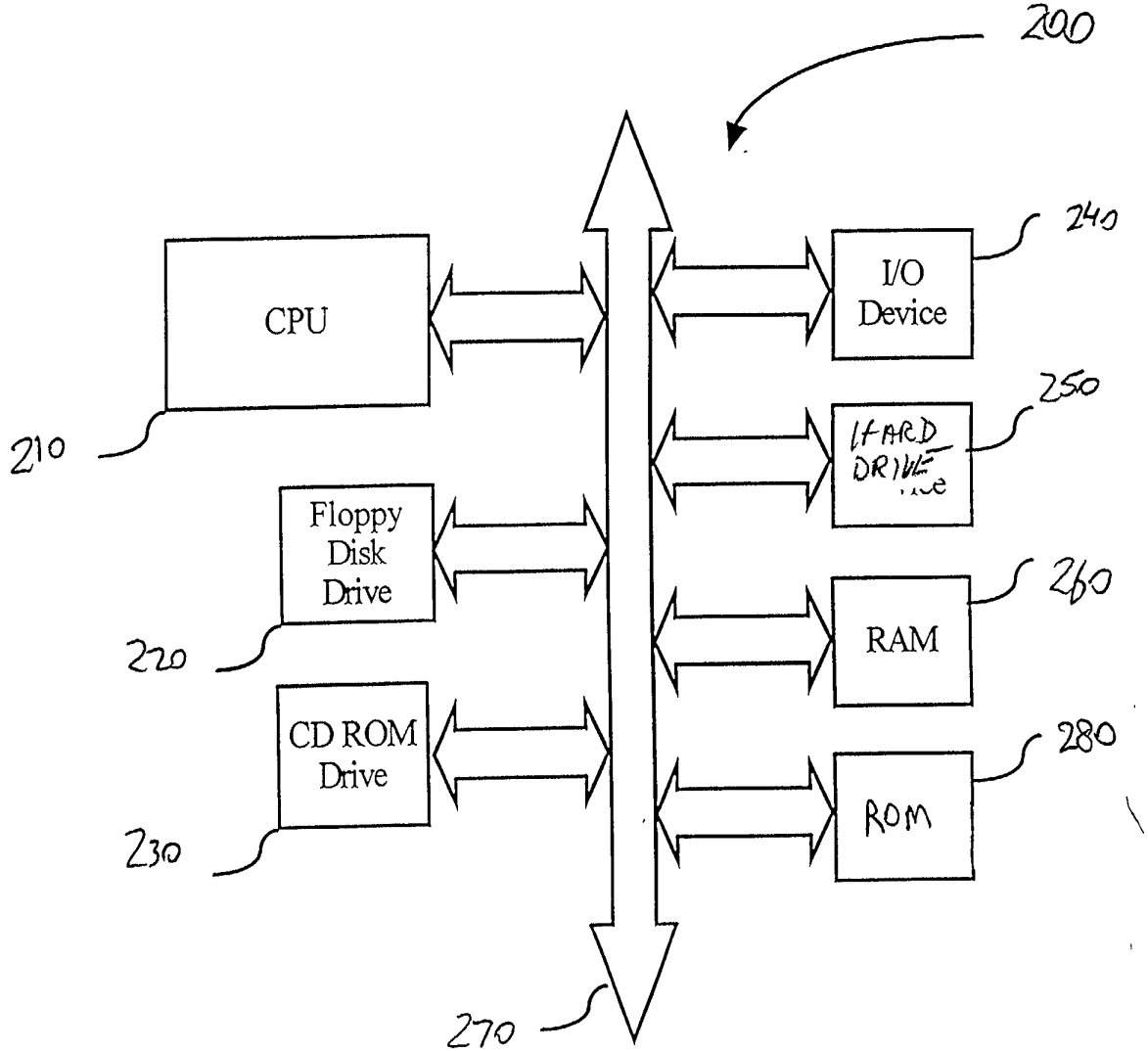
200
CPU
210
Floppy Disk Drive
220
CD ROM Drive
230
I/O Device
240
HARD DRIVE
250
RAM
260
ROM
280
270

Fig. 5

Docket No.: M4065.0244/P244
Micron No.: 99-0700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND APPARATUS FOR ADJUSTING DATA HOLD TIMING OF AN OUTPUT CIRCUIT

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code
§ 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to Thomas J. D'Amico of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street NW, Washington, DC 20037-1526. Telephone calls should be made to (202) 785-9700.

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Docket No.: M4065.0244/P244
Micron No.: 99-0700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

Signature Page for Second Inventor

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Docket No.: M4065.0244/P244
Micron No.: 99-0700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
James Cullum et al.

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Filed Herewith

Examiner: Not Yet Assigned

For: METHOD AND APPARATUS FOR ADJUSTING DATA HOLD TIMING OF AN OUTPUT CIRCUIT

Assistant Commissioner for Patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Micron Technology, Inc., Assignee of the entire right, title and interest in the above-identified application by virtue of the Assignment attached hereto (which is also being submitted concurrently for recordation), hereby appoints the attorneys and agents of the firm of located at , listed as follows: Gary M. Hoffman, 26,411; Thomas J. D'Amico, 28,371; Donald A. Gregory, 28,954; James W. Brady Jr., 32,115; Jon D. Grossman, 32,699; Mark J. Thronson, 33,082; Jeremy A. Cubert, 40,399; Laurence E. Fisher, 37,131; Brian A. Lemm, 43,748; John F. Levis, 34,210; Gianni Minutoli, 41,198; Edwin Oh, P-45,319; Eric Oliver, 35,307; William E. Powell III, 39,803; Paul L. Ratcliffe, 45,290; Mark E. Strickland, 45,138 and Salvatore P. Tamburo, P-45,153, and also attorneys of Micron Technology, Inc. as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The Assignee certifies that the above-identified assignment has been reviewed and to the best of the Assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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